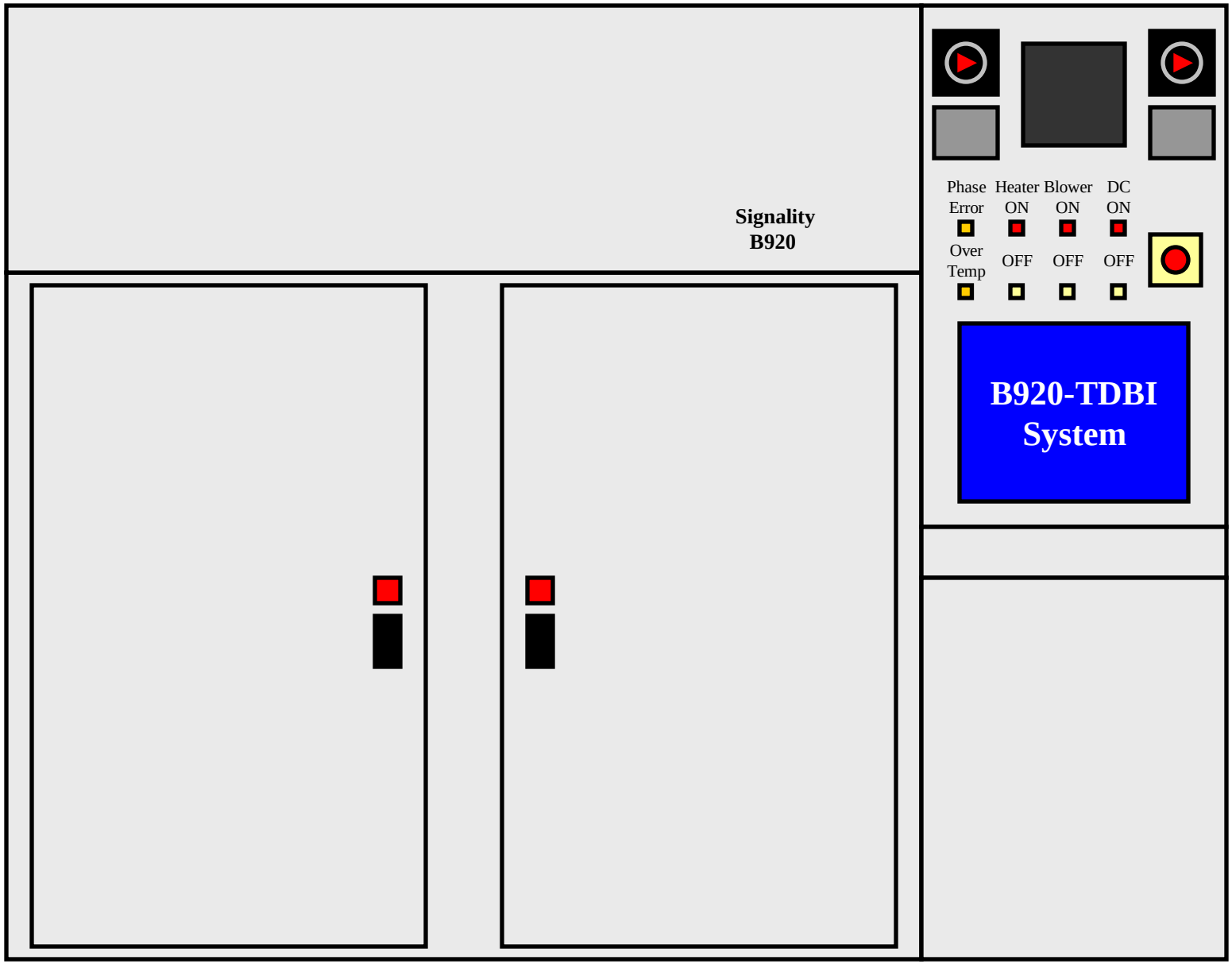
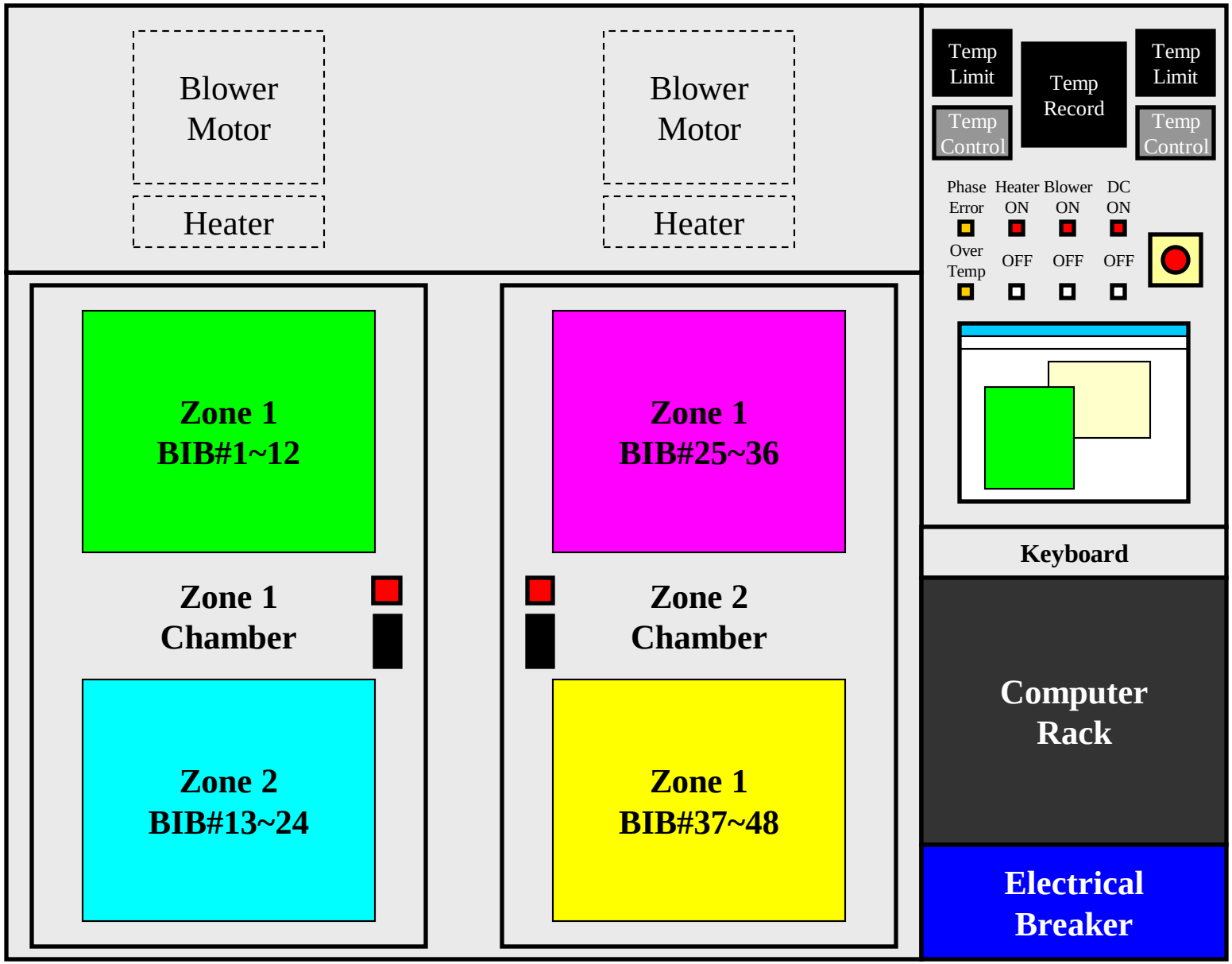
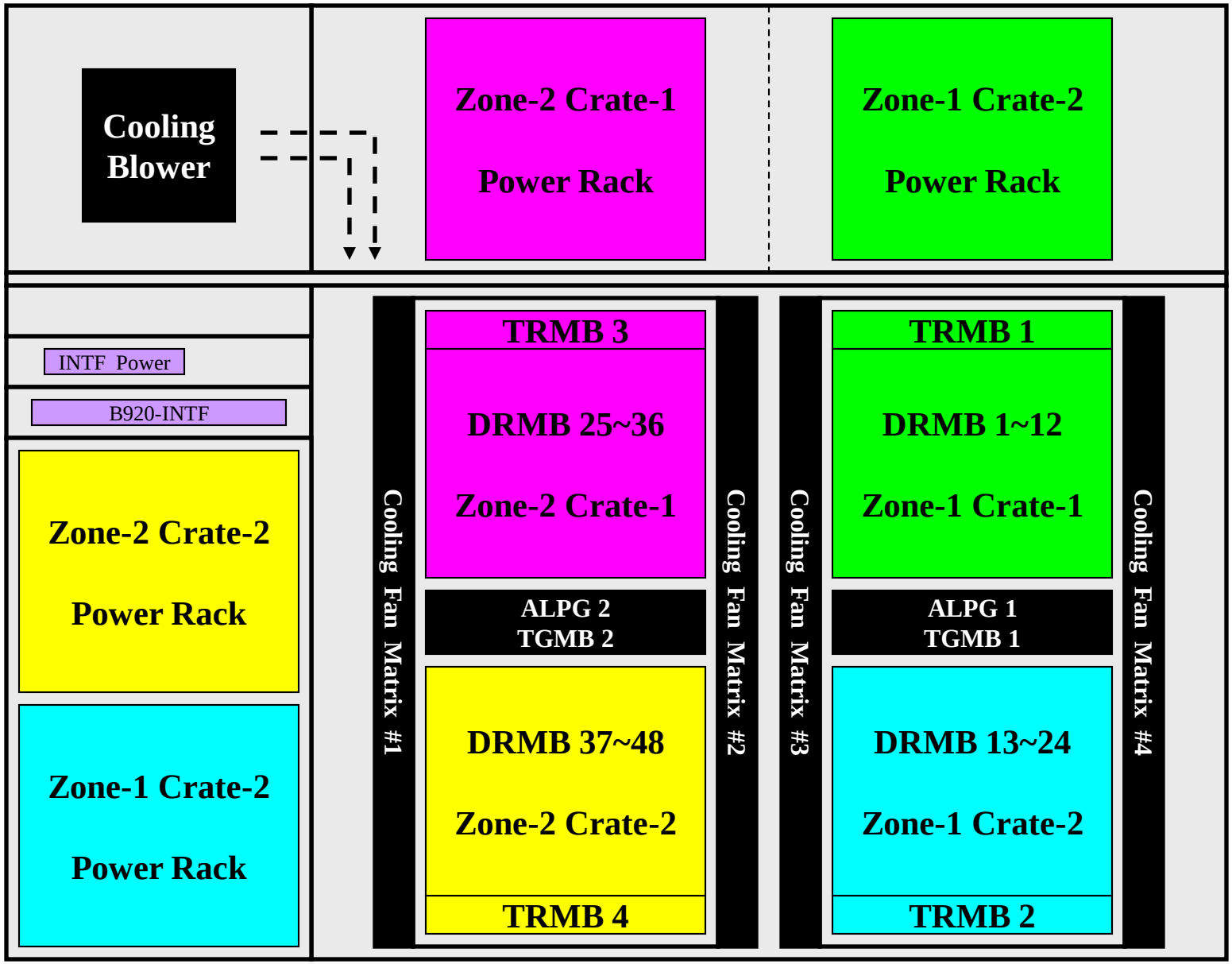
B920 System Outline



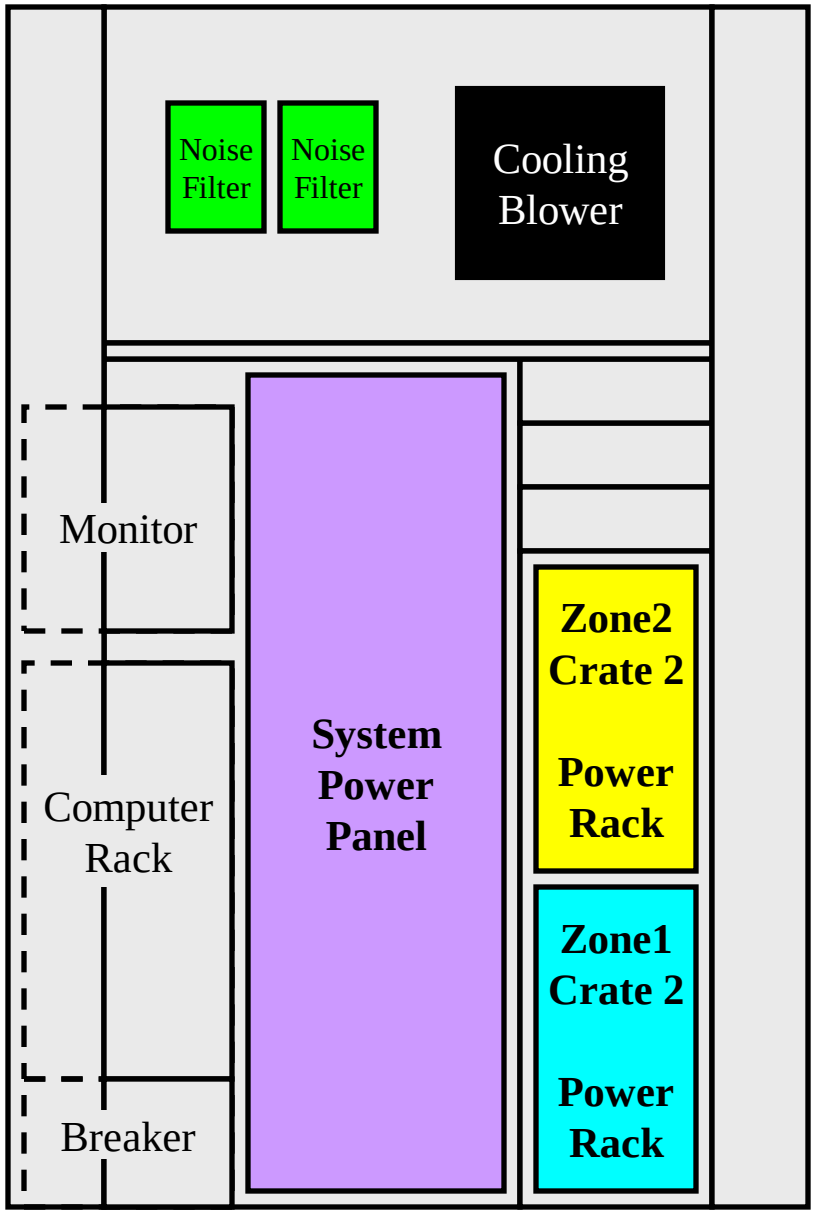
B920 System Front View



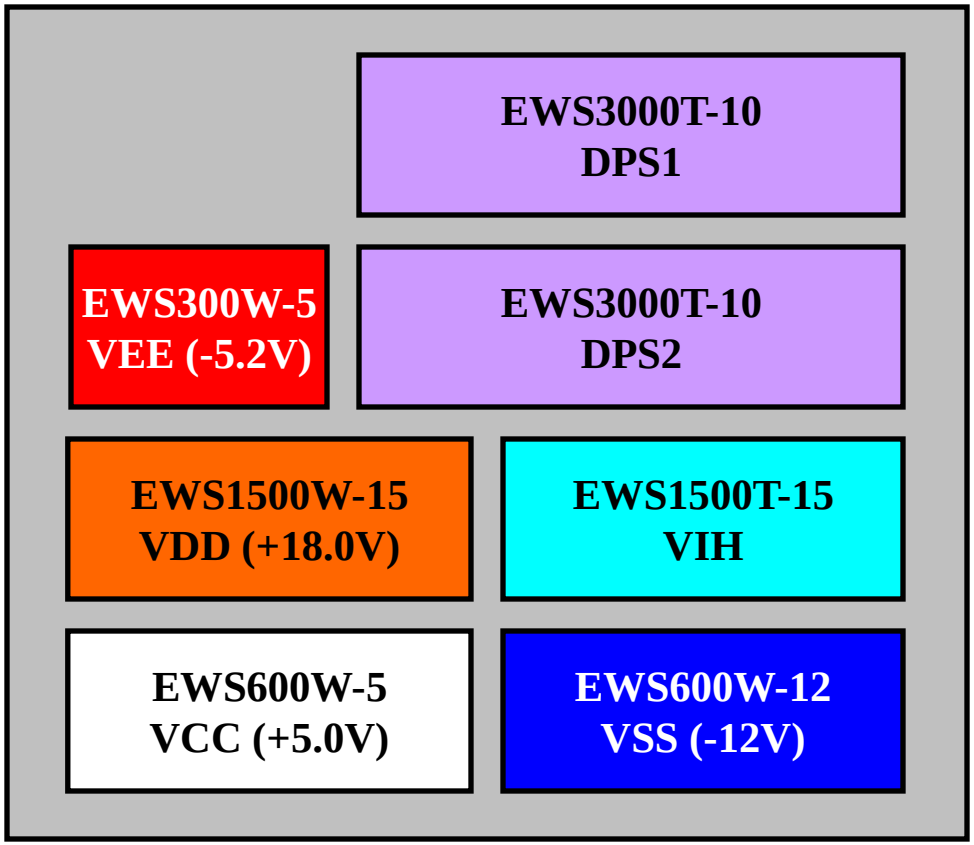
B920 System Rear View



B920 System Right Side View

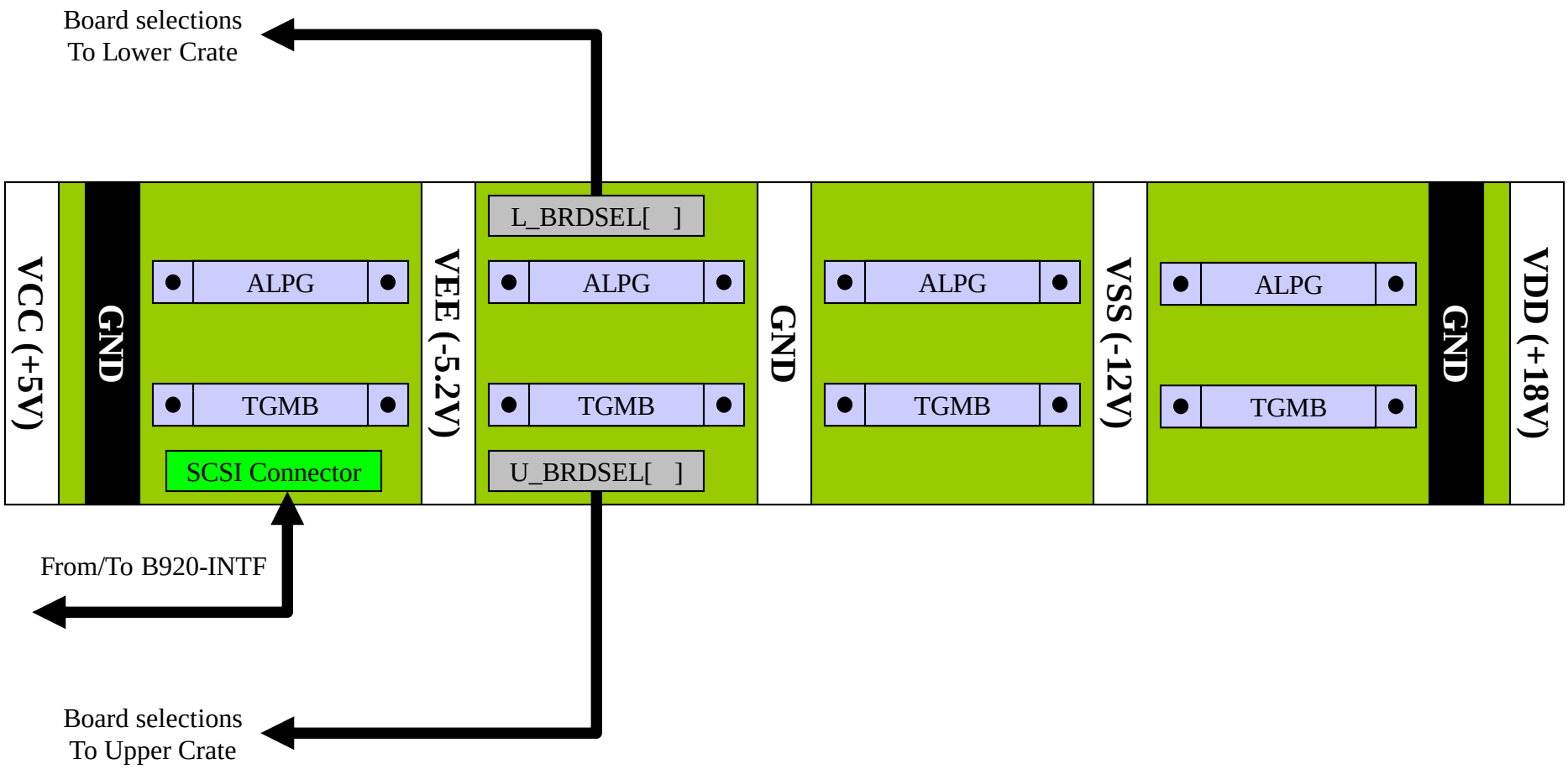


B920 Power Rack

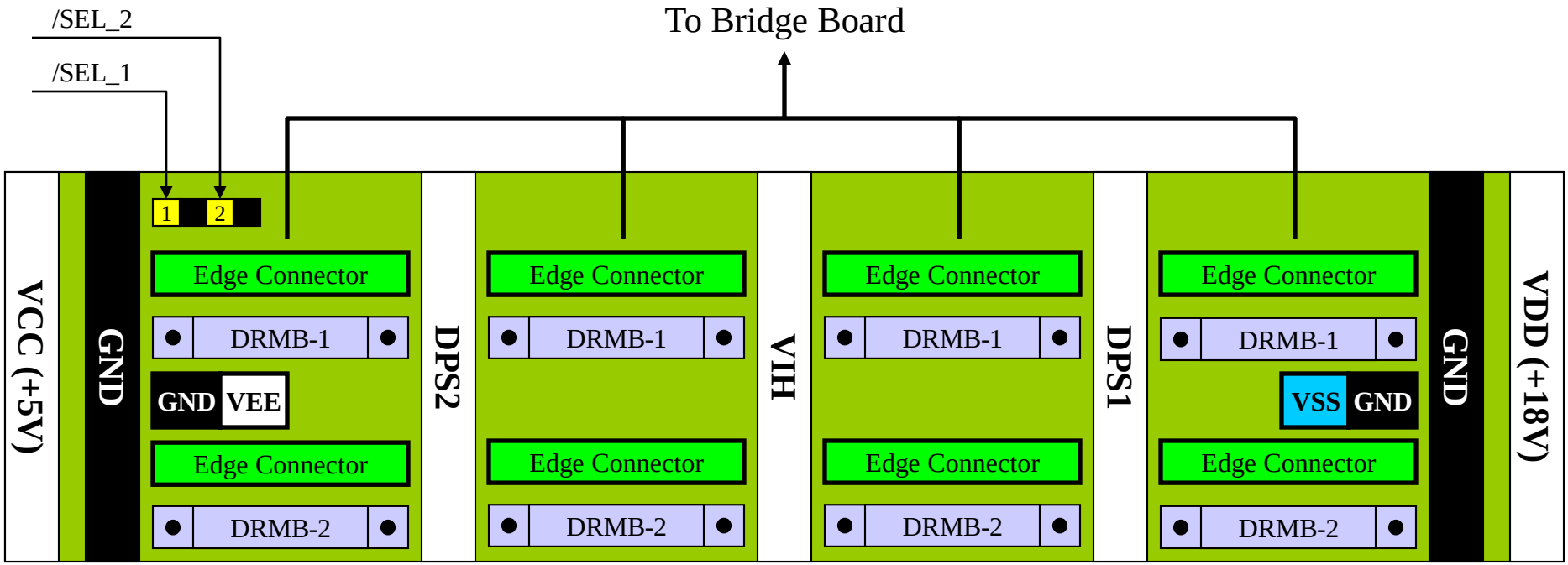


	Control	Power Supply Name
System Power	B920-INTF	VCC / VEE /VDD /VSS
Burn-In Use	B920-TRMB	DPS1 / DPS2 / VIH

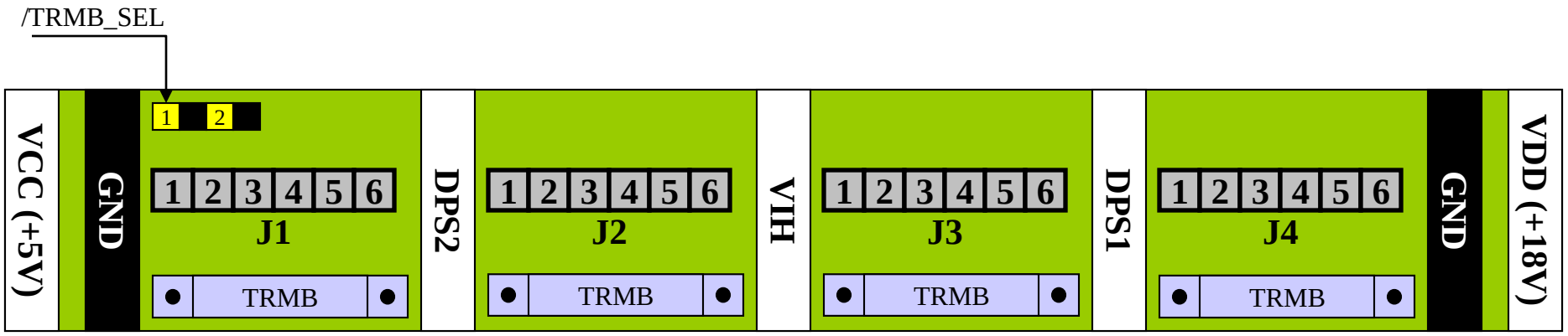
TGMB Back Plane(TGBK) View



DRMB Back Plane(DRBK) View



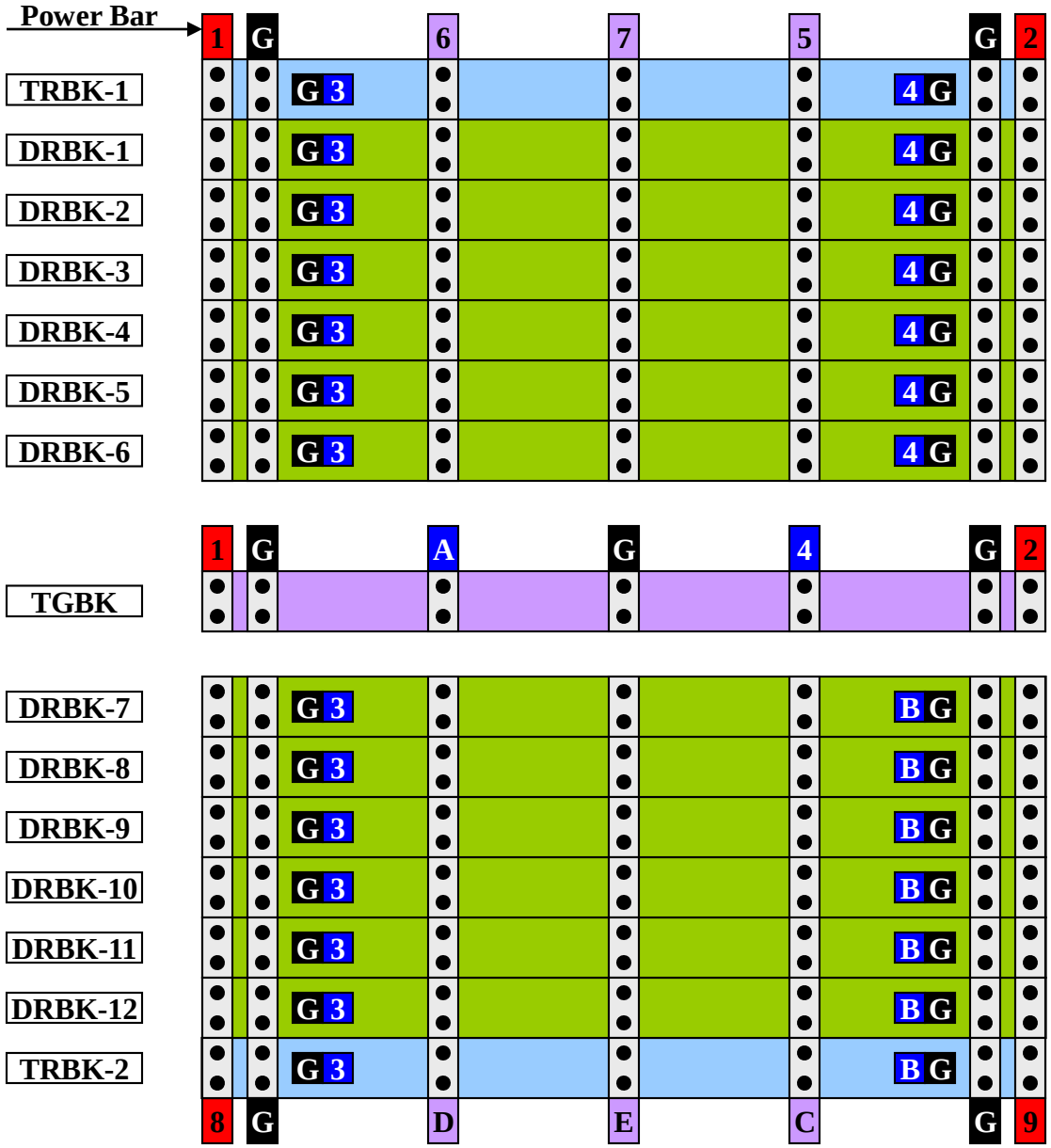
TRMB Back Plane(TRBK) View



	1	2	3	4	5	6
J1	GND	VEE	DPS1_PV	GND	DPS1_CNT	DPS1_TOG
J2	DVM+	DVM-	SPA1	SPB1	SPA2	SPB2
J3	DPS2_PV	GND	DPS2_CNT	DPS2_TOG	VIH_PV	GND
J4	VIH_CNT	VIH_TOG	SPA3	SPB3	VSS	GND

VSS / VEE	GND	TRMB –12V/-5.2V Power Terminals
XXX_PV	GND	To EWS3000T-10/1500T-15 Power supply PV Terminals.
XXX_CNT	XXX_TOG	To EWS3000T-10/1500T-15 Power supply CNT/TOG Terminals.
DVM+	DVM-	For calibration use only.
SPAx	SPBx	Reserved. NC

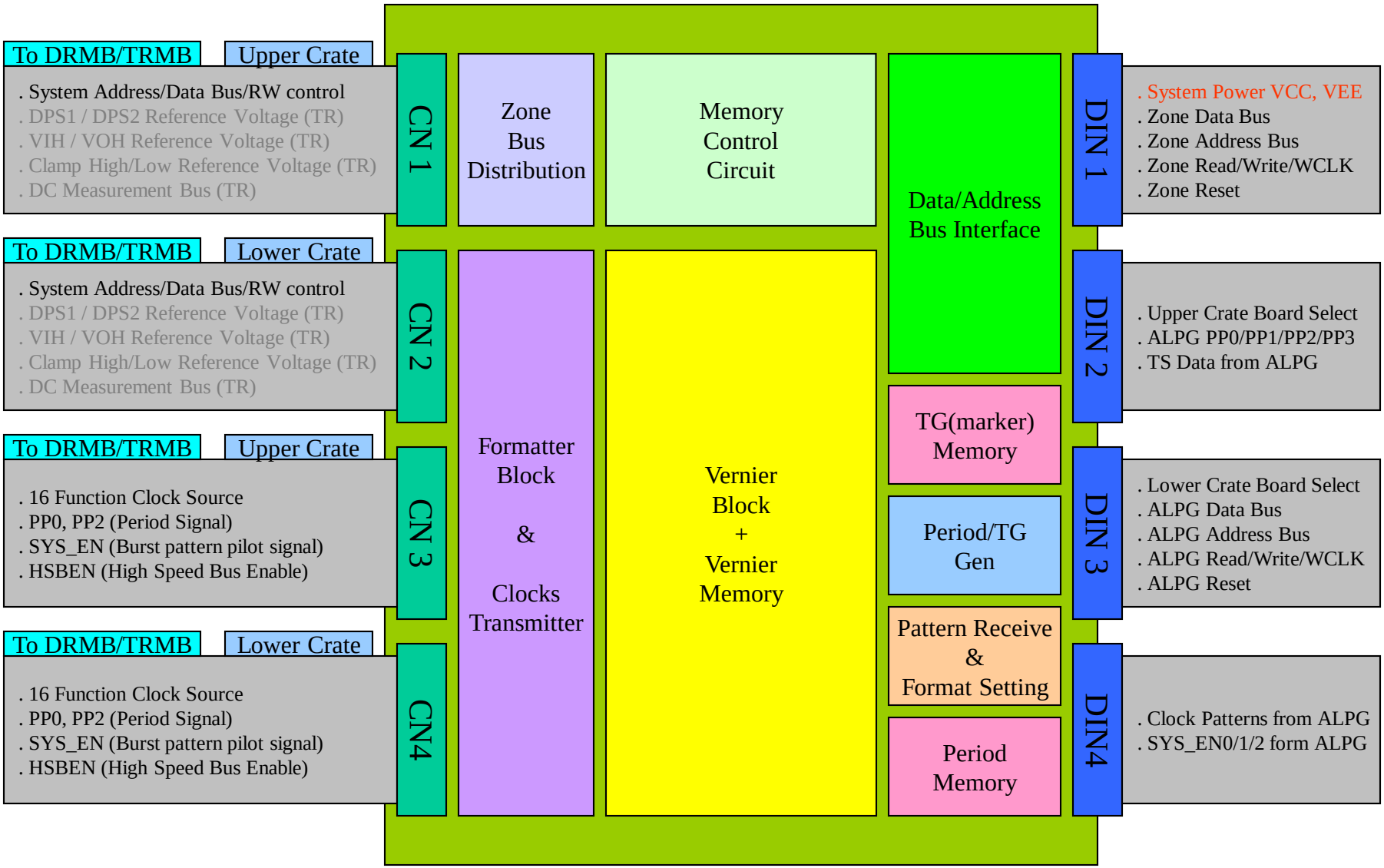
Zone Power Connection



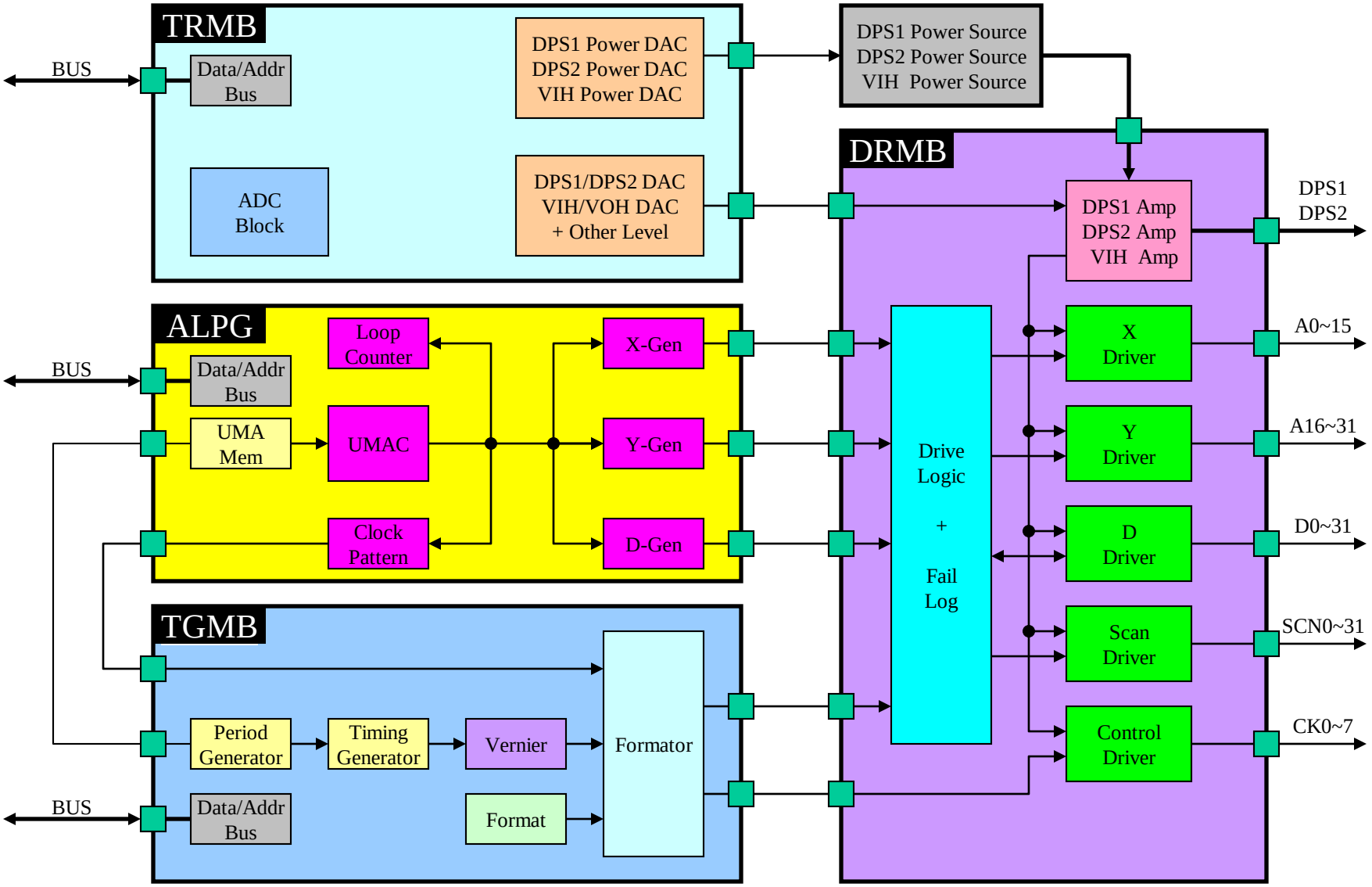
1	VCC – Crate 1
2	VDD – Crate 1
3	VEE – All Zone
4	VSS – Crate 1
5	DPS1 – Crate 1
6	DPS2 – Crate 1
7	VIH – Crate 1

8	VCC – Crate 2
9	VDD – Crate 2
A	VEE – TGMB/ALPG
B	VSS – Crate 2
C	DPS1 – Crate 2
D	DPS2 – Crate 2
E	VIH – Crate 2

B920 TG Board Overview



B920 System Functional Block



TG Board Main Function

System Zone Data/Address Bus Distribution

- Upper Crate Data/Addr Bus , R/W/CLK & RST
- Lower Crate Data/Addr Bus , R/W/CLK & RST
- ALPG Data/Addr Bus , R/W/CLK & RST

Zone Driver Board Board Selection

- DRMB#1~12 Selection
- TRMB#1 Selection
- ALPG Selection
- DRMB#13~24 Selection
- TRMB#2 Selection

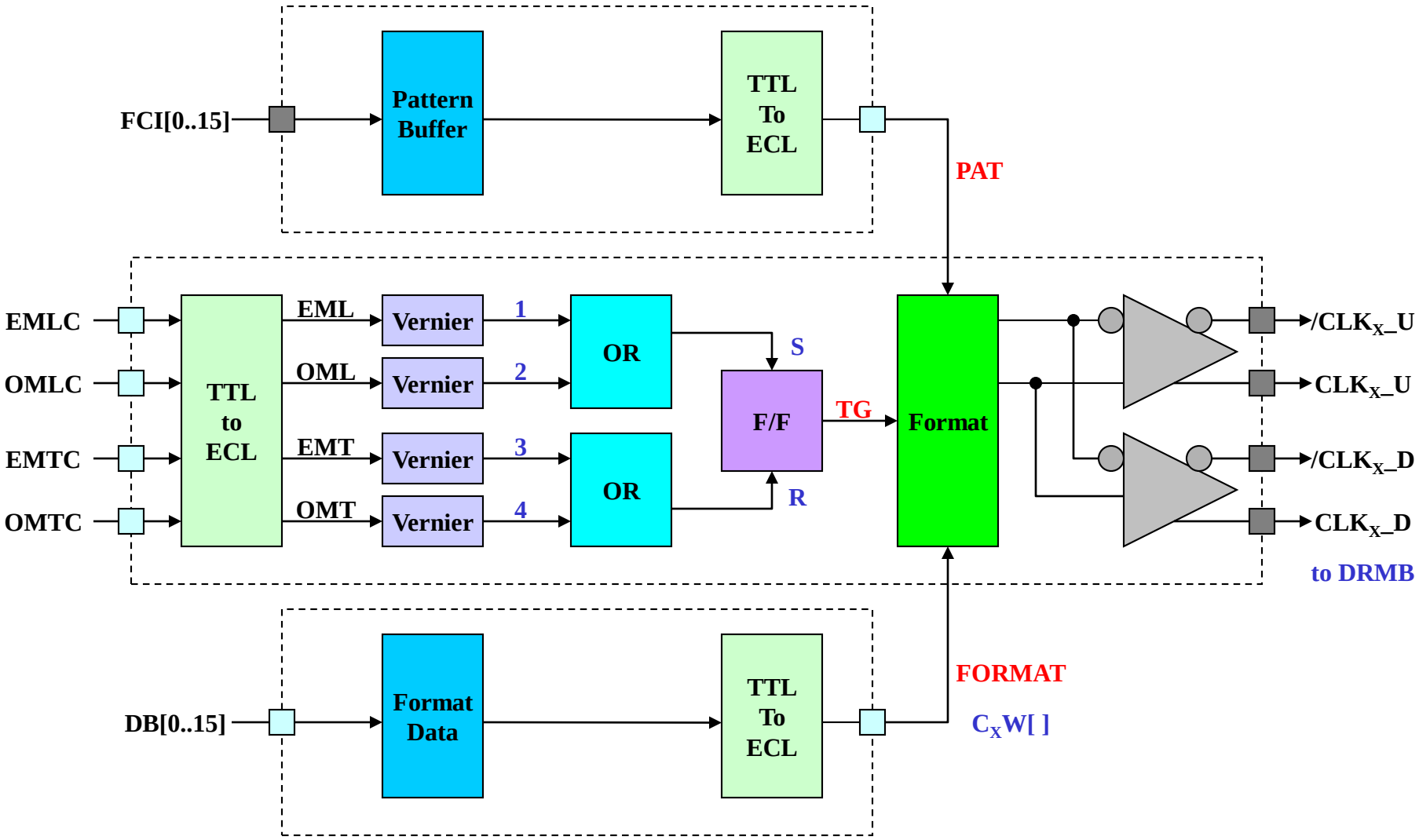
Provide Driver Board with 8 User define Controlled Source.

- Clock_0~7

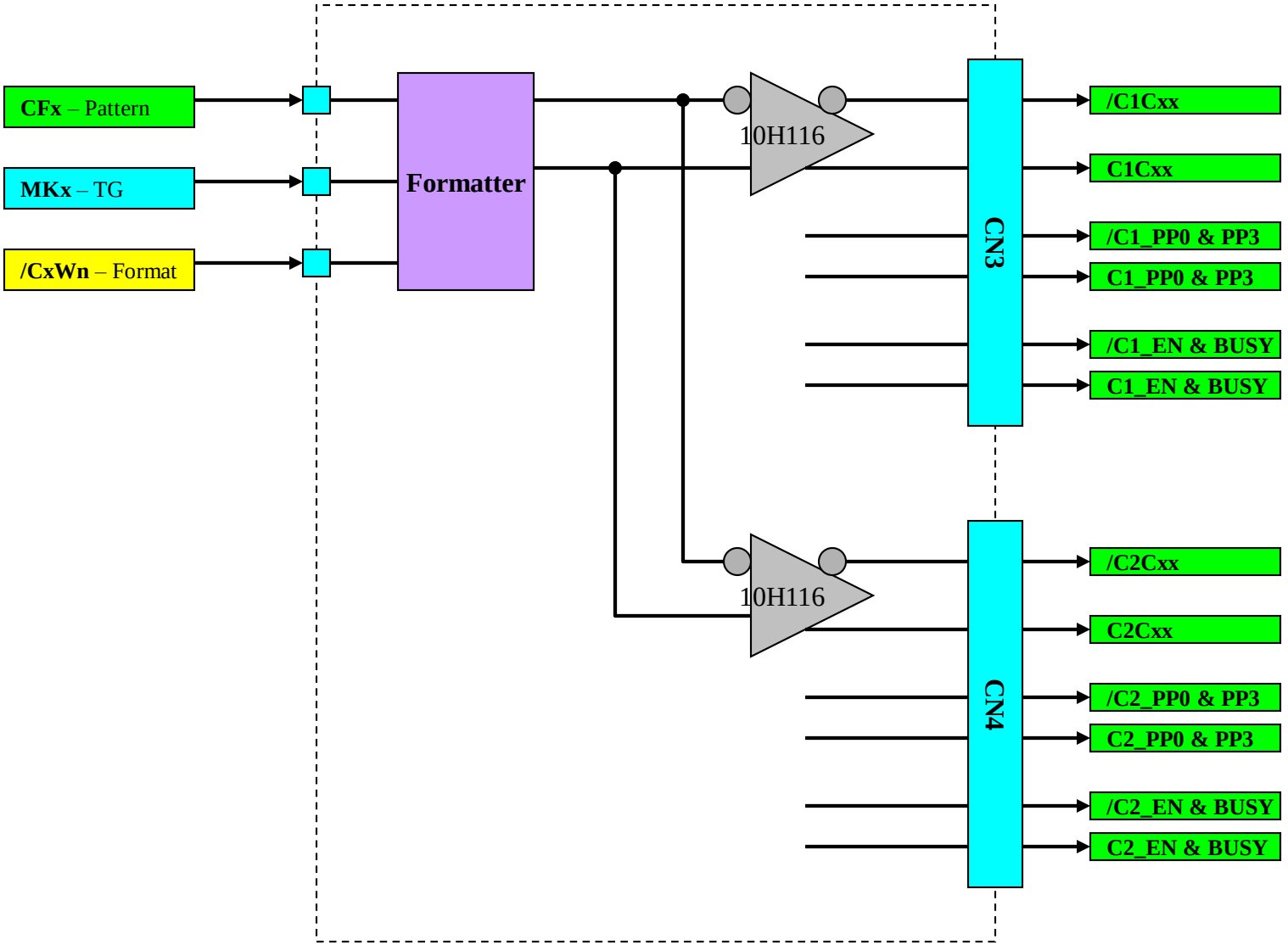
Provide Driver Board with 8 Functional Clock Source

- DEN Clock
- AMUX Clock
- DINV Clock
- XINV Clock
- YINV Clock
- SCAN1 Clock
- SCAN2 Clock
- Strobe Clock

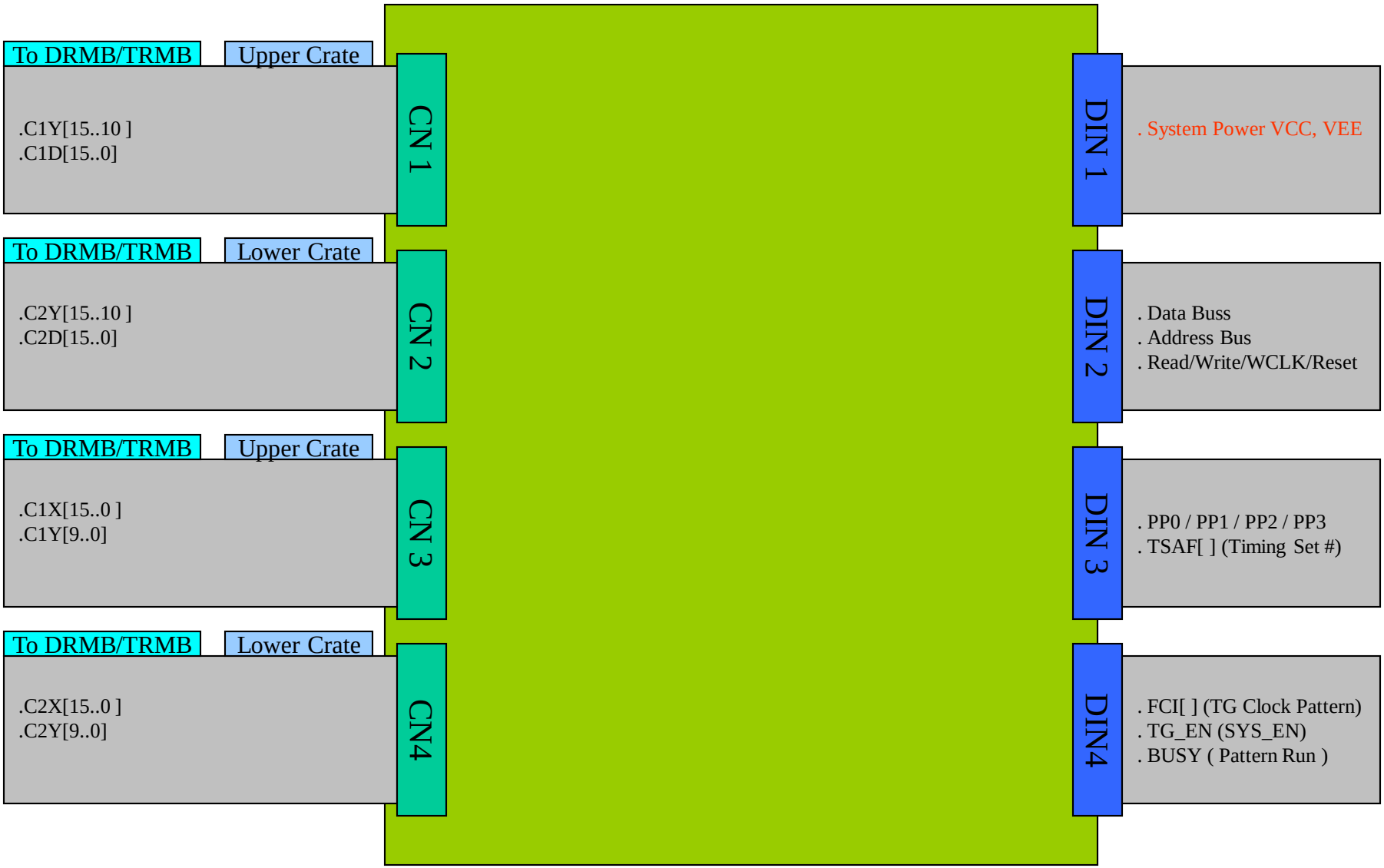
TG Signal Flow



TG Signals Transmission



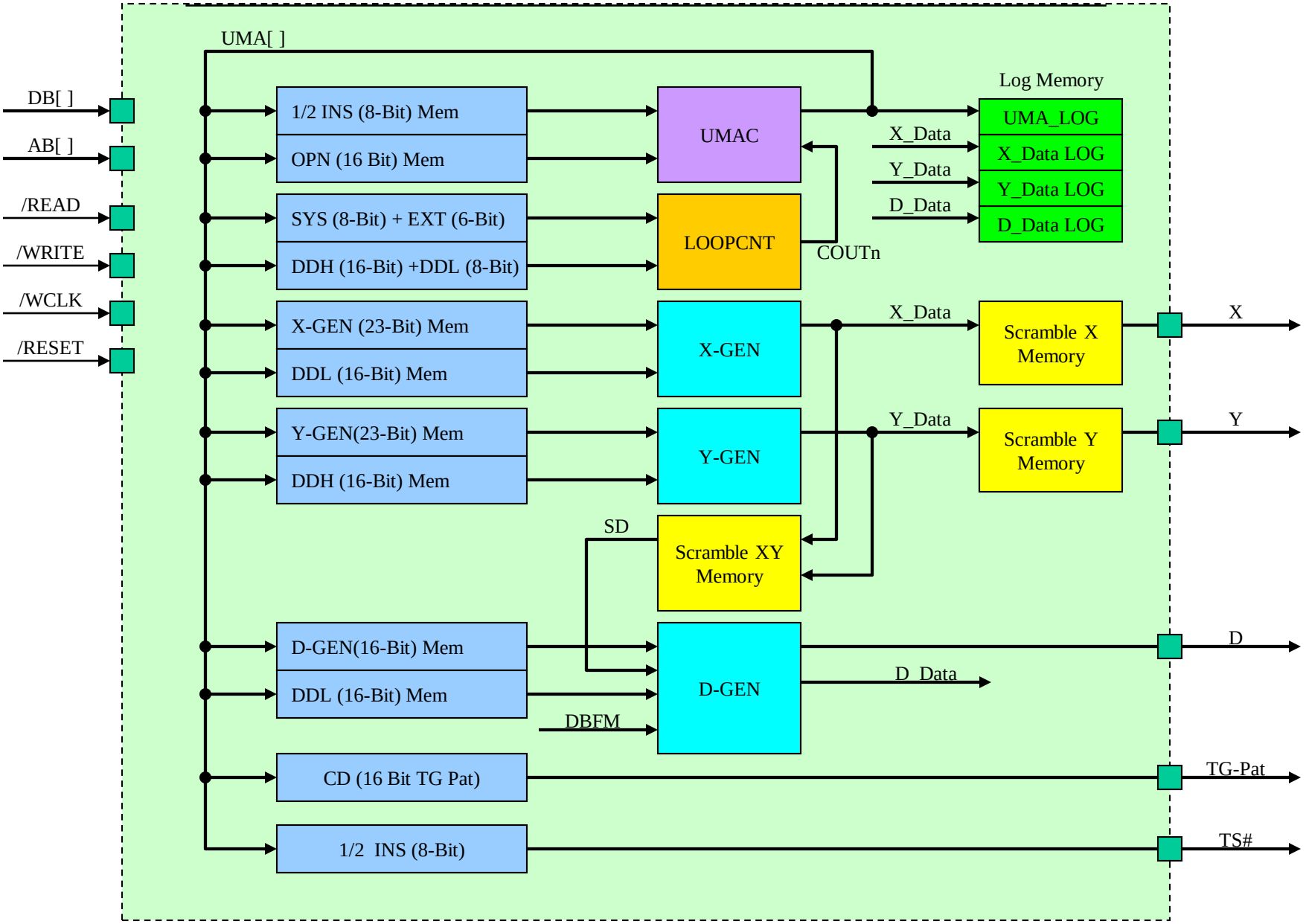
B920 ALPG Overview



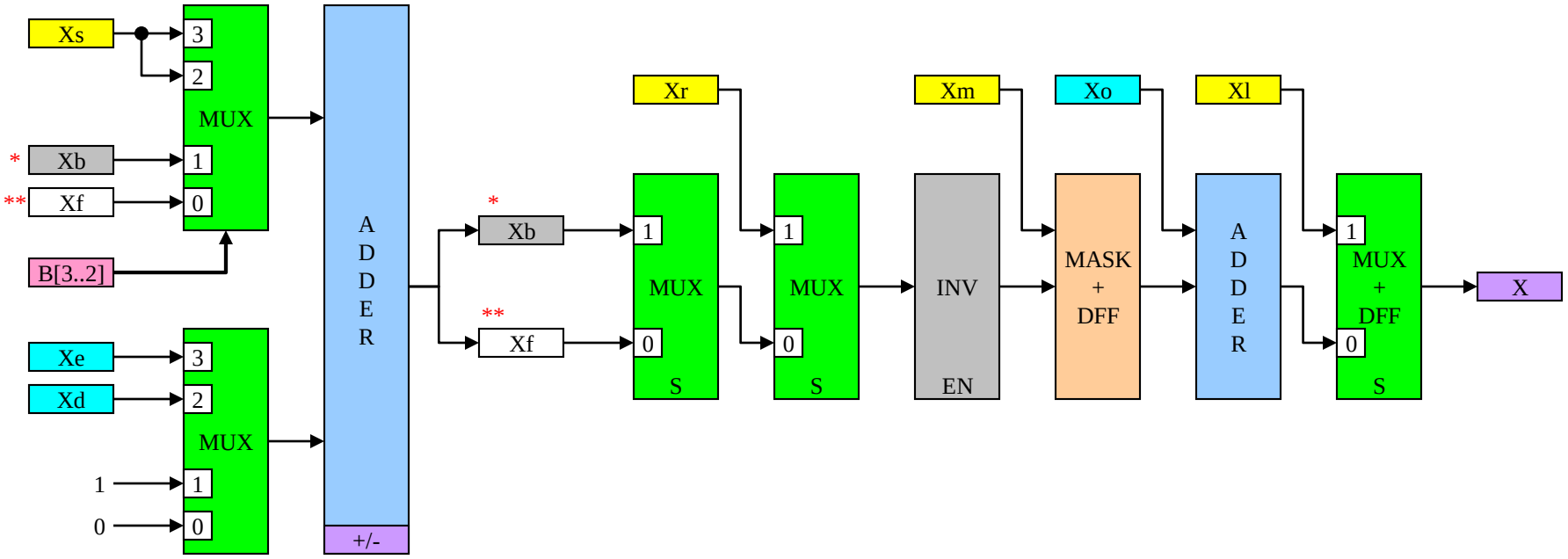
B920 ALPG Main Function

1. Pattern Sequence Control (UMAC).
2. DUT X-Address Pattern Generation(X-Gen).
3. DUT Y-Address Pattern Generation(Y-Gen).
4. DUT D Pattern Generation(D-Gen).
5. Provide the Patterns for user controlled clock pins.
6. Provide 8 Loop-Counters For Pattern Test Application.

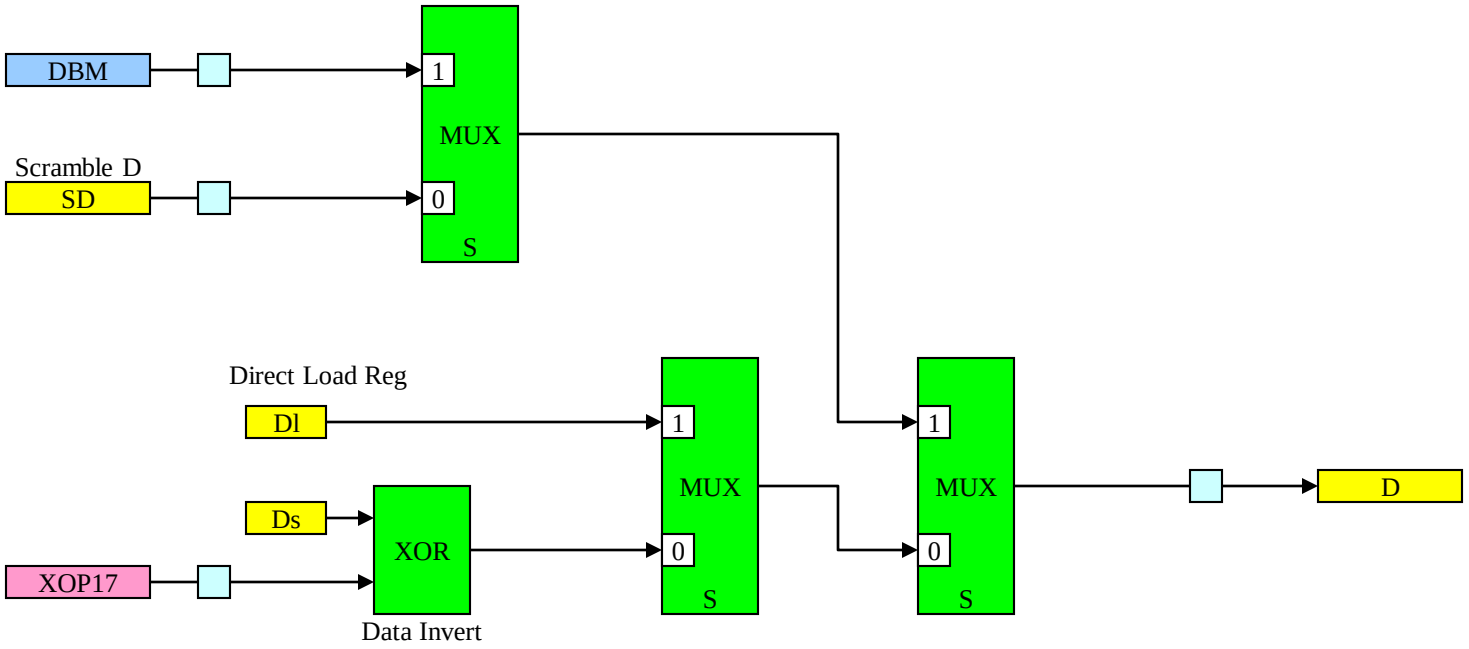
B920 ALPG Main Functional Block



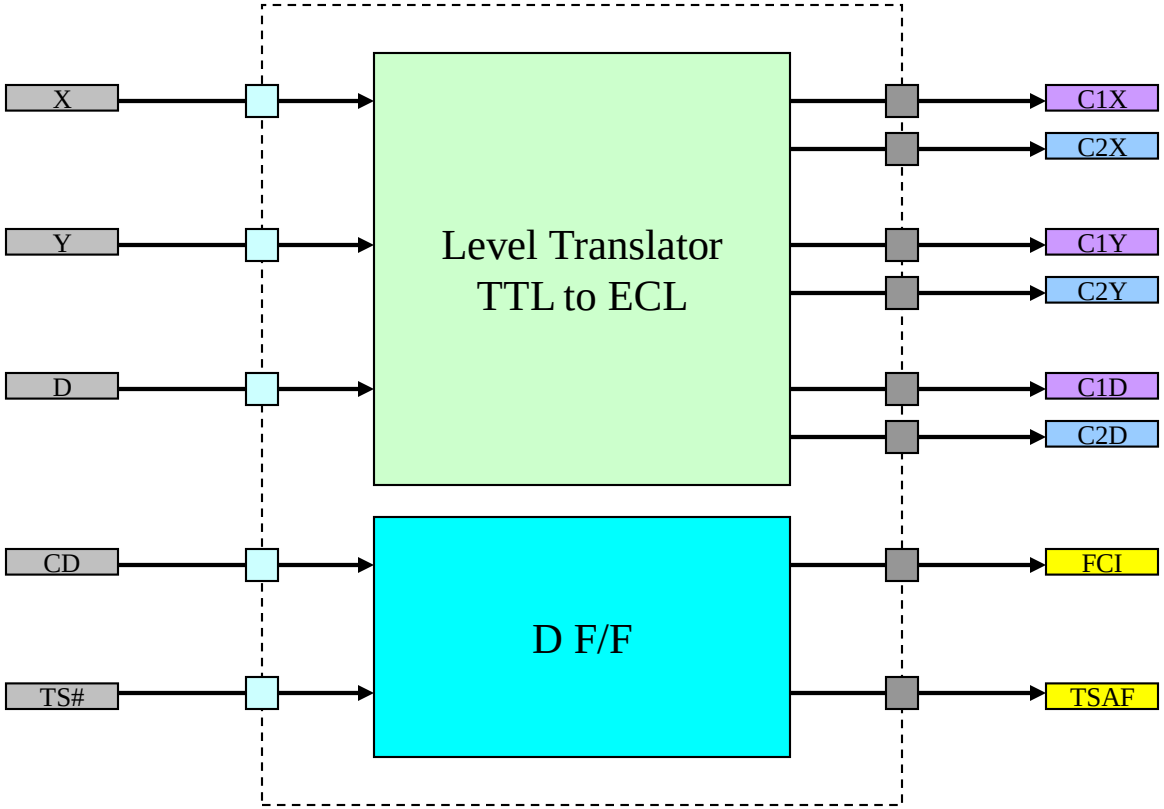
X/Y Gen Block


Xs
3
2
MUX
*
Xb
1
**
Xf
0
B[3..2]
Xe
3
Xd
2
MUX
1
1
0
0
A
D
D
E
R
+/-
*
Xb
**
Xf
Xr
1
MUX
0
S
1
MUX
0
S
Xm
INV
EN
Xo
MASK
+
DFF
Xl
A
D
D
E
R
1
MUX
+
DFF
0
S
X

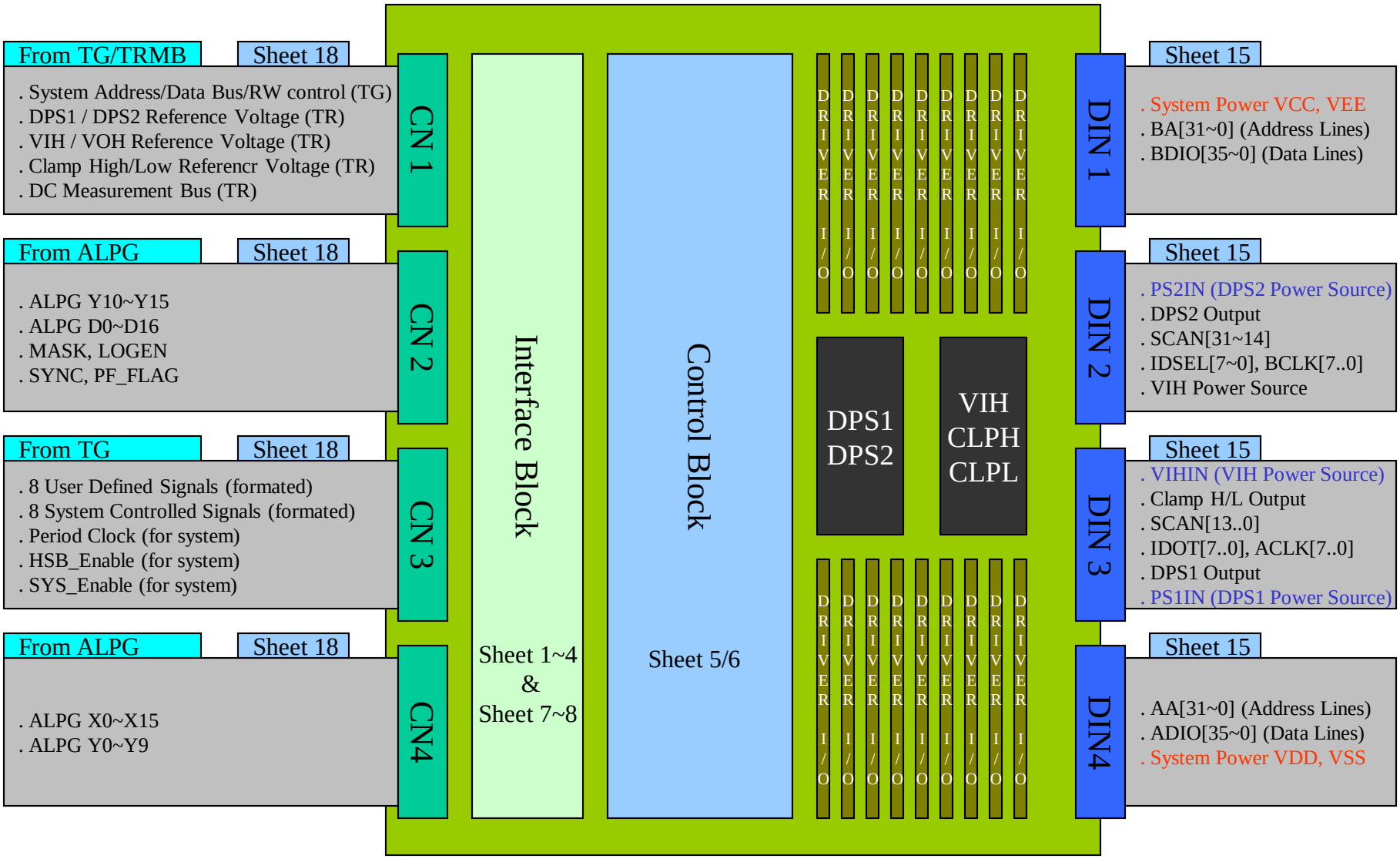
D Gen Block


DBM
1
MUX
Scramble_D
SD
0
S
Direct Load Reg
Dl
1
MUX
1
MUX
D
Ds
XOR
0
0
XOP17
S
S
Data Invert

Output Stage



B920 Driver Board Overview



CN1 Signals

. System Address/Data Bus/RW control (From/To TG) ------ TTL level

- System Address Bus (AB1, AB2, AB3, AB4, AB5, AB15).
- System Data Bus (DB0~DB15).
- Read/Write/Clock/Reset (/RB, /WB, /RST, /WCB).

. PS1F / PS2F / VIHF /VOHF Reference Voltage (from TR)

- DPS1/DPS2 setting Value for Burn-In Board Device.
- Driving level for logic 1 and Output Threshold level.

. CLPHF / CLPLF Reference Voltage (fromTR)

- Clamp High / Clamp Low Level for signal ringing shaping.

. PS1I_PKT / PS2I_PKT / VIHI_PKT Referencr Voltage (from TR)

- Max Current setting level for DPS1 / DPS2 and VIH power.

. DC Measurement Bus (To TR)

- For DC Resource Monitor or Calibration.

CN2/4 Signals

. XYD Patterns Signals ------ ECL level

- X Address patterns (CNX0~15).
- Y Address Patterns (CNY0~15).
- D Data Patterns (CND0~15).
- All are ECL level and differential signals.

. MASK / LOG / SYNC / PF (From/To ALPG) ------ ECL level

- Comparision Mask (CNMASK).
- Log Enable (CNLOG).
- Synchronous Signal (CNSYNC)
- Pass/Fail Flag (CNPF)
- All are ECL level and differential signals.

CN3 Signals

. CLK Signals ------ ECL level

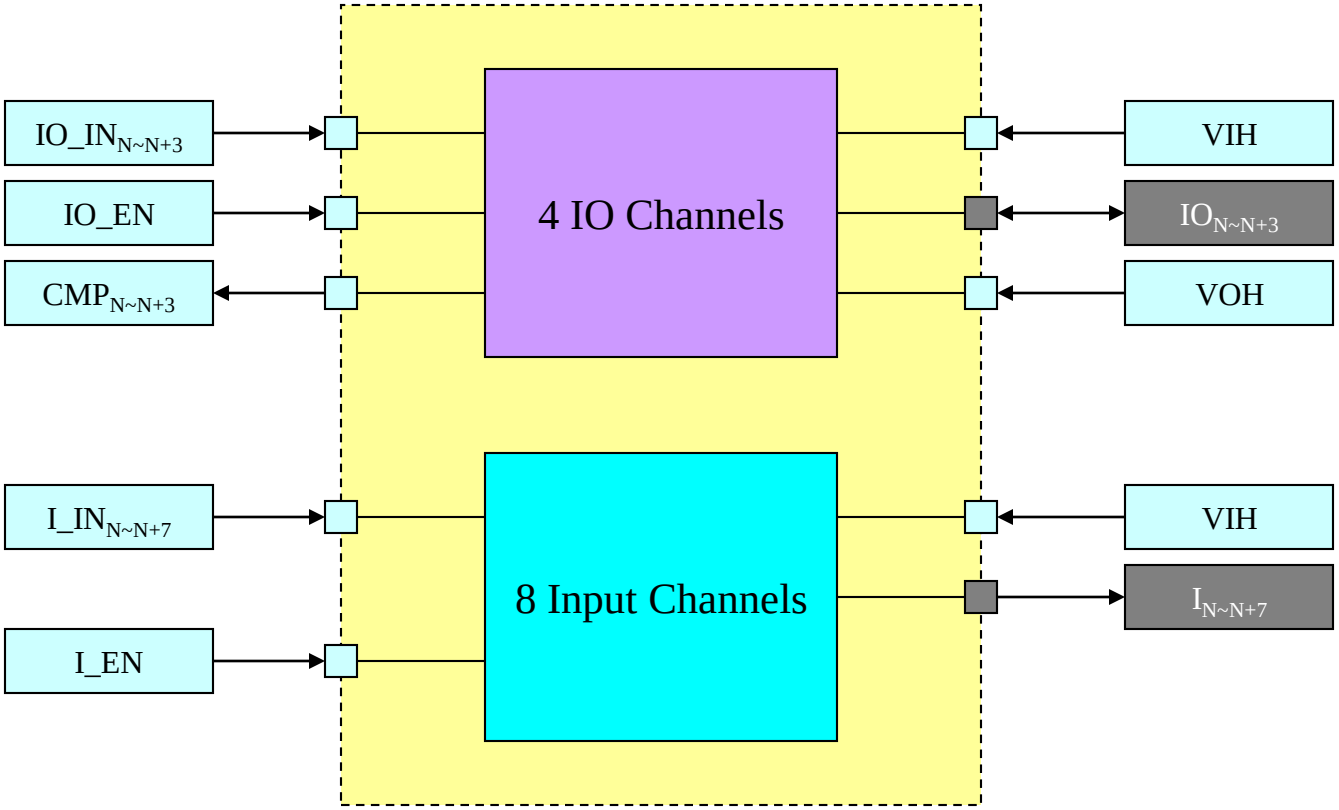
- Dedicated CLK (CNC0~7).
- User defined CLK (CNC8~15).
- All are ECL level and differential signals.

. PP0 / PP3 / SYS_EN / HSBEN ------ ECL level

- Period Start T0 (CNCPP0).
- Period Start with delay 3 TGCLK (CNCPP3).
- System Enable Signal (CNCEN).
- High Speed Bus Enable (CNBUSY)
- All are ECL level and differential signals.

Driver I/O Card

Total 18 Driver Cards on DRMB, 9 for set A, 9 for set B.



Digital Portion

. Register Read/Write Control
- DPS1/DPS2/VIH Amp ON/OFF
- DC Measurement select
- Driver Signals Gating Control
- DC Resources Offset Compensation

. BIB ID# Reading Control
- IDSEL0~7
- IDOT0~7

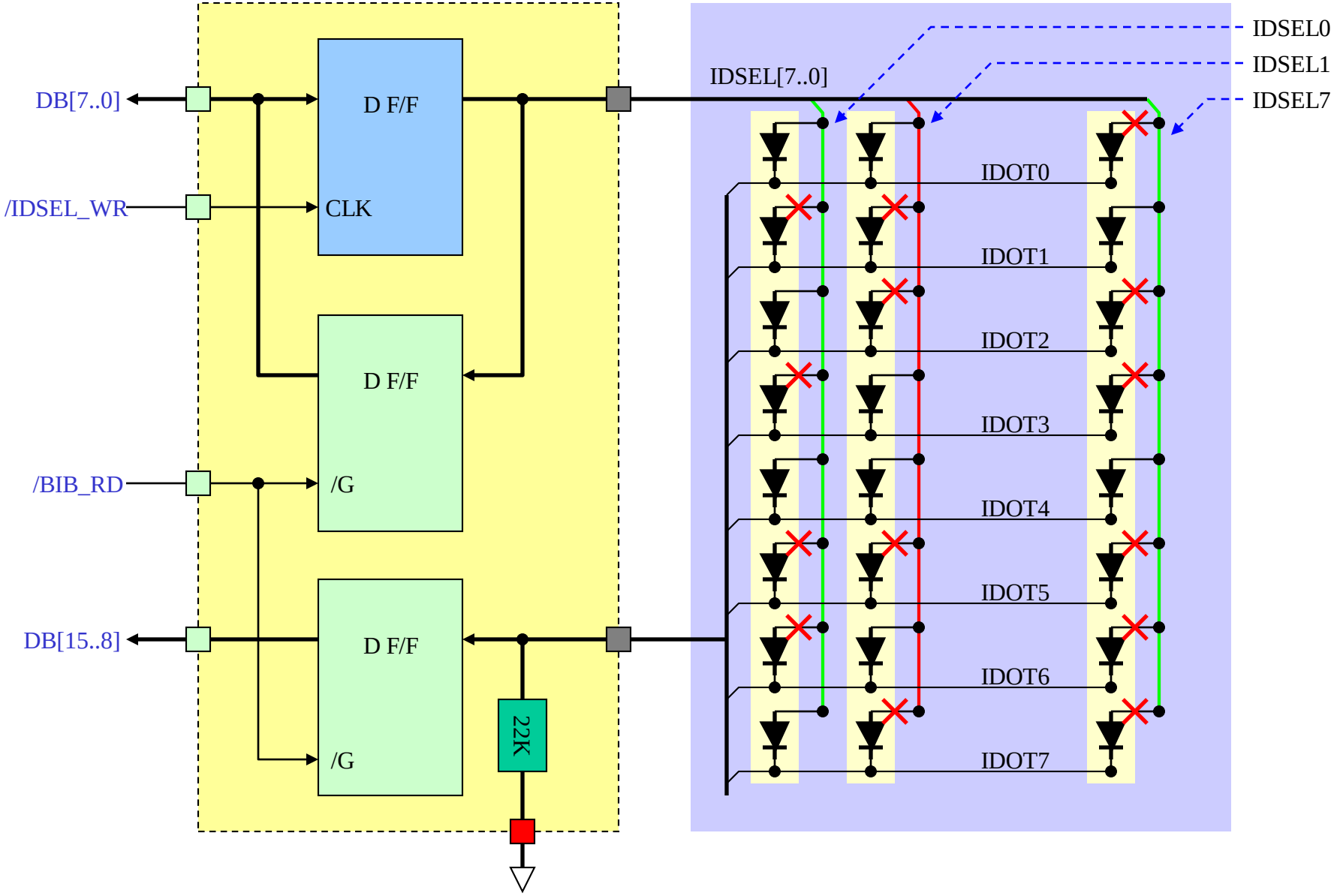
. Function Chip – B9DM8K1
- 4 I/O Channels
- 4 Scan Channels
- 2 X-Addr Channels
- 2 Y-Addr Channels

. Fail Memory Controllor – B9DM8K2
- Fail Memory Address
- Fail Memory Banks Read/Write/Enable Control

. Fail Memory

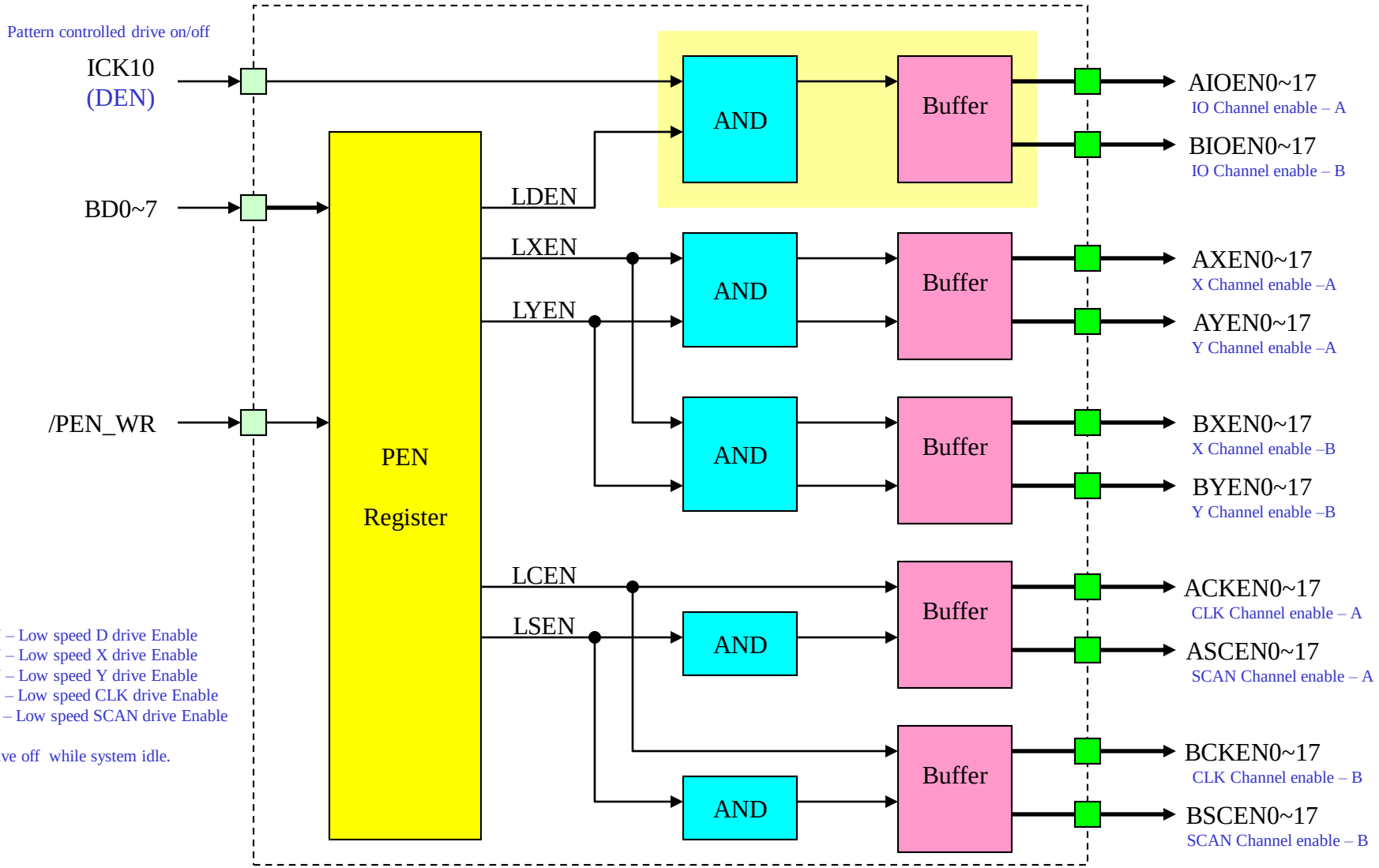
IDSEL & IDOT

Burn-In Board ID#



Drive Signal Gating

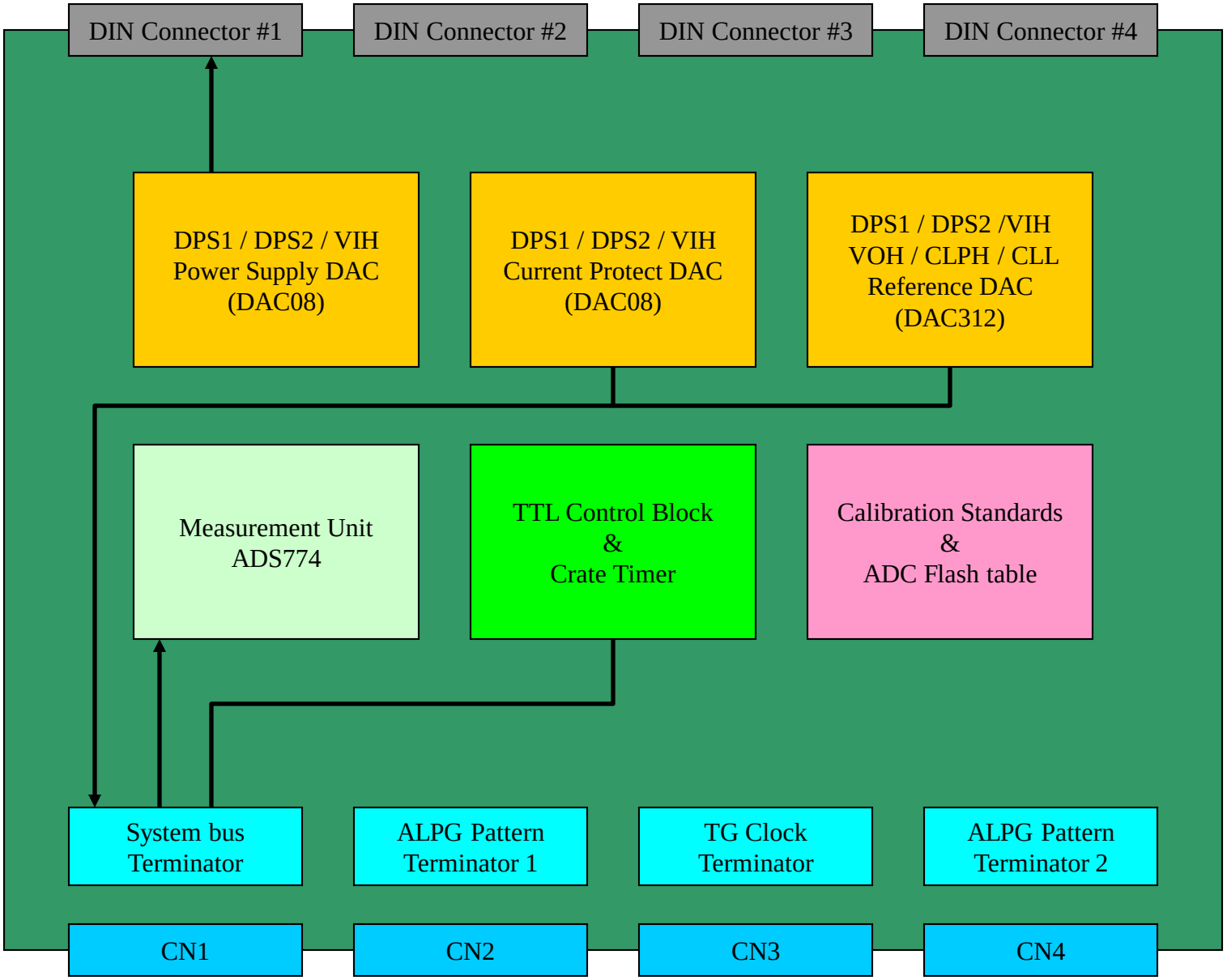
: To Driver Cards



1. LDEN – Low speed D drive Enable
2. LXEN – Low speed X drive Enable
3. LYEN – Low speed Y drive Enable
4. LCEN – Low speed CLK drive Enable
5. LSEN – Low speed SCAN drive Enable

6. All drive off while system idle.

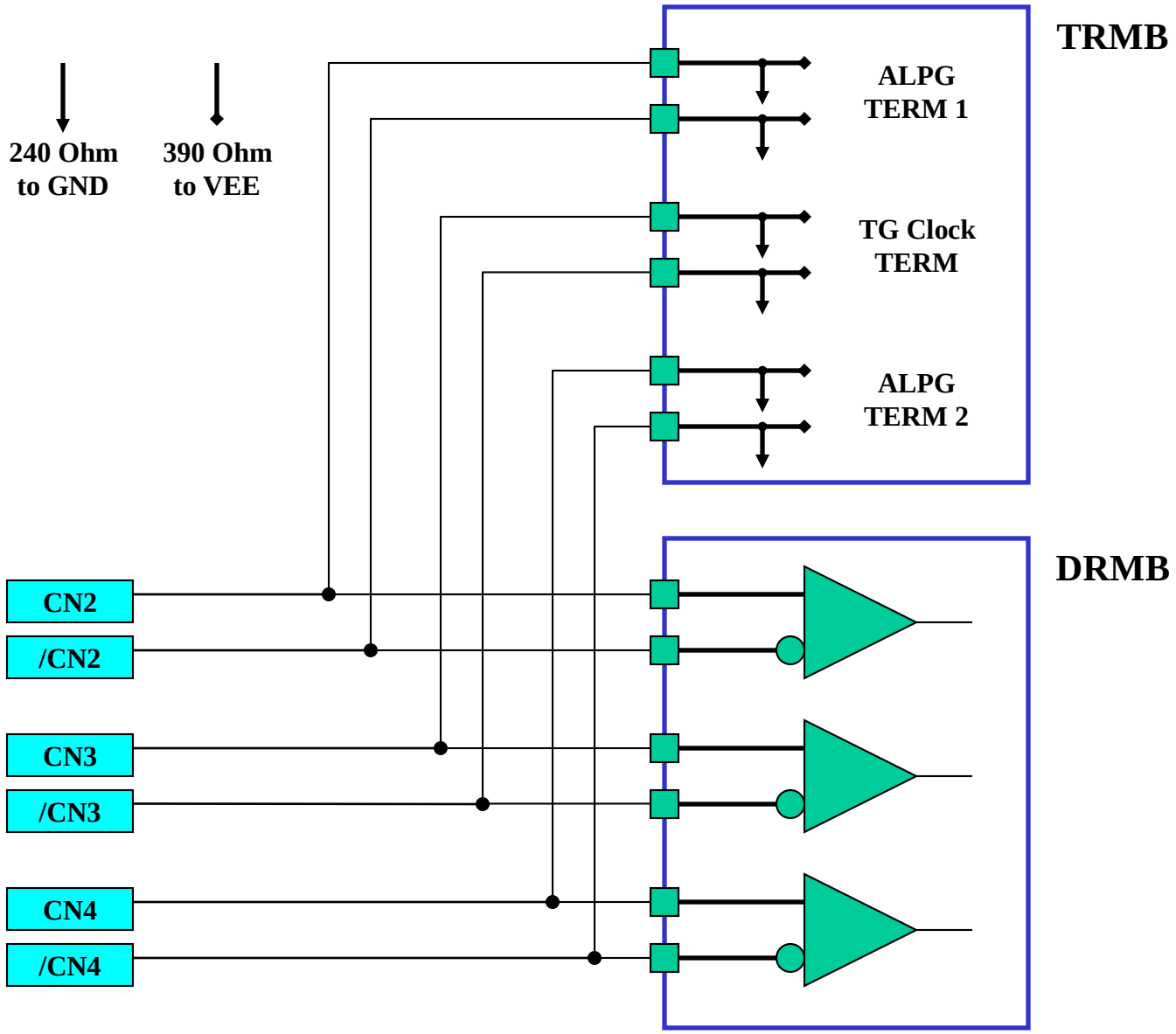
TRMB Block Diagram



TRMB (Termination Board) Main Function

- System Bus Termination
- TG Clock Signals Termination
- ALPG Pattern Signals Termination
- DPS1, DPS2,VIH Power Supply Control
- DPS1, DPS2, VIH Current Protection Control
- DPS1, DPS2 Reference Value Control
- VIH, VOH Reference Value Control
- Clamp High/Low Reference Voltage Control
- DC Resource Measurement
- DC Calibration Standard Voltage Sources
- Timer Function

TRMB ECL Termination



TRMB / DRMB DC Connection